Customer No.: 31561
Application No.: 10/707,015
Docket NO.: 10542-US-PA

AMENDMENT

In the Claims:

Claim 1 (original) A process for fabricating a substrate, at least comprising the steps of

providing a semi-finished substrate having a plurality of insulating layers and a plurality of patterned metallic layers alternately stacked over each other, wherein the patterned metallic layers are electrically interconnected, the two outermost insulating layers in the semi-finished substrate are defined as a first insulating layer and a second insulating layer, two inner patterned metallic layers are defined as a first patterned metallic layer and a second patterned metallic layer, the first insulating layer and the second insulating layer cover the first patterned metallic layer and the second patterned metallic layer respectively, and the first insulating layer and the second insulating layer have a plurality of first openings and a plurality of second openings that expose the first patterned metallic layer and the second patterned metallic layer respectively;

forming a first seed layer on the first insulating layer and in the first openings and forming a second seed layer on the second insulating layer and in the second openings;

forming a first mask layer and a second mask layer over the first seed layer and the second seed layer and patterning the first mask layer and the second mask layer to form a plurality of first patterned openings and a plurality of second patterned openings, wherein the first patterned openings and the second patterned openings expose the first openings and the second openings respectively;

depositing a first metal and a second metal into the first openings and the second openings to form a first metallic layer and a second metallic layer respectively, wherein the first metallic layer and the second metallic layer are positioned over the first seed layer and the second seed layer, and the second metallic layer is partially filled into the second patterned opening in the second mask layer;

removing the first mask layer and the second mask layer;

forming a third mask layer over the first seed layer and the first metallic layer and forming a fourth mask layer over the second seed layer and the second metallic layer, wherein the third mask layer has a plurality of third patterned openings that exposes the first seed layer and the first metallic layer;

forming a plurality of circuit lines inside the third patterned openings such that the circuit lines are positioned over the first seed layer and the first metallic layer;

removing the third mask layer and the fourth mask layer;

removing the exposed first seed layer and the second seed layer;